Notice of Allowability	Application No.	Applicant(s)	
	10/693,285	YANG, HONDA	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed 10/23/2003*.

2. ☒ The allowed claim(s) is/are *1-4 and 6-11, renumbered (37 C.F.R. 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 12/08/2005.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *12/08/2005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

VUTHE SIEK
PRIMARY EXAMINER

DETAILED ACTION

1. This office action is in response to the Application 10/693,285 filed 10/23/2003.

2. Claims 1-20 are pending in the Application.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-4, 6-11, drawn to a method and structure for application specific integrated circuit (ASIC), including ASIC partitioning and prototyping it with FPGAs, classified in class 716, subclass 8.

II. Claims 5, 12-20, drawn to a method and structure for application specific integrated circuit and prototyping it with FPGA, classified in class 716, subclass 8.

4. The inventions are distinct, each from the other because of the following reasons:

5. Inventions Group II and Group I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because a block of an application specific integrated circuit being prototyped. The subcombination has

separate utility such as a partitioning an application specific integrated circuit into multiple programmable logic devices.

6. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with Forrest Gunnison (Registration No. 32,899) on 12/05/2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-4, 6-11. Affirmation of this election must be made by applicant in replying to this Office action. Claims 5, 12-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

EXAMINER'S AMENDMENT

8. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

9. Authorization for this examiner's amendment was given in a telephone interview with Forrest Gunnison (Registration No. 32,899) on 12/08/2005.

10. The application has been amended as follows:

To Drawings

11. The following changes to the drawings have been approved by the examiner and agreed upon by applicant: figures 5, 6 and 7 have to be changed: on the figure 5

vague numbers and letters need to be replaced to make it clear; figures 6 and 7 heed to be split into 2-3 parts to make them bigger and readable. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

To claims

12. Claims 5, 12-20 are cancelled from the Application as non-elected claims.

Claim 1 line 3 delete "placing" insert –programming--

Claim 1 line 7 delete "placing" insert –programming--

Claim 2 line 30 after "created" insert --, wherein n is an integer--

Claim 6 line 9 after "signals" insert --, wherein said block of said application specific integrated circuit was programmed in said first programmable logic device--

Claim 6 line 17 after "prototyped" insert --, wherein said another block of said application specific integrated circuit was programmed in said first programmable logic device--

Allowable Subject Matter

13. Claims 1-4, 6-11 are allowed. The following is an examiner's statement of reasons for allowance: Applicant is disclosing a method and structure for application specific integrated circuit prototyping, wherein the application specific integrated circuit is partitioned into programmable blocks, and each partitioned block of the application specific integrated circuit is programmed in each programmable logic device (first programmable logic device and second programmable logic device), wherein in order to communicate with each other each partitioned block coupled to COM wrapper

containing serializer and deserializer units for converting plurality of parallel output signals to a serial data stream and from serial data stream to the plurality of parallel output signals as claimed.

14. While these elements are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ***ipsissimis verbis*** *test, i.e., identity of terminology is not required.* ***In re Bond,*** *910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

15. In particular, the prior art does not teach the specific arrangement of elements including partitioning the application specific integrated circuit into blocks (partitions), wherein each partition (block) of the application specific integrated circuit is programmed (prototyped) by programmable logic device, including connecting each partition (block) to it's own COM wrapper for converting plurality of parallel output signals to a serial data stream and back from serial data stream to the plurality of parallel output signals for communication between partitions (blocks) of the application specific integrated circuit; wherein each COM wrapper contains serializer or deserializer.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McCubbrey (US Patent Application Publication 20040060032) discloses an automated system and method for programming FPGAs for implementing user-defined algorithm specified in a high level language, including substituting ASIC by FPGAs with the development of an image processing algorithm or other sequence of desired operations into the birstream coding required to program FPGAs, but lacks the specific arrangement of elements including partitioning the application specific integrated circuit into blocks (partitions), wherein each partition (block) of the application specific integrated circuit is programmed (prototyped) by programmable logic device, including connecting each partition (block) to it's own COM wrapper for converting plurality of parallel output signals to a serial data stream and back from serial data stream to the plurality of parallel output signals for communication between partitions (blocks) of the application specific integrated circuit; wherein each COM wrapper contains serializer or deserializer. Brophy et al. (US Patent 6,892,337) discloses a system for testing a physical layer device or various network portions connected to that physical layer device, wherein any physical layer devices can be deployed as a programmable logic device (PLD) replacing ASIC including serializer/deserializer for testing the seralizer and deserializer functions of the physical layer interface at the normal operating speed at which the seral data stream is produced from the serializer and received by the deserializer, but lacks the specific arrangement of elements including partitioning the application specific integrated circuit into blocks (partitions),

wherein each partition (block) of the application specific integrated circuit is programmed (prototyped) by programmable logic device, including connecting each partition (block) to it's own COM wrapper for converting plurality of parallel output signals to a serial data stream and back from serial data stream to the plurality of parallel output signals for communication between partitions (blocks) of the application specific integrated circuit; wherein each COM wrapper contains serializer or deserializer. Lesea et al. (US Patent 6,496,971) discloses an FPGA containing an on-chip processor, that reads configuration data onto the FPGA and controls the loading of that configuration data into FPGA including converting a serial bitstream into parallel output signals, but lacks the specific arrangement of elements including partitioning the application specific integrated circuit into blocks (partitions), wherein each partition (block) of the application specific integrated circuit is programmed (prototyped) by programmable logic device, including connecting each partition (block) to it's own COM wrapper for converting plurality of parallel output signals to a serial data stream and back from serial data stream to the plurality of parallel output signals for communication between partitions (blocks) of the application specific integrated circuit; wherein each COM wrapper contains serializer or deserializer. Douglass et al. (US Patent 6,798,239) discloses interconnecting logic for providing connectivity of an embedded fixed logic circuit or circuits with programmable logic fabric including substituting ASIC by FPGA, wherein a specific implementation of an interface logic is used having multiplexers for serializing parallel data of signals to serial data and demultiplexers to convert serial data into parallel data, but lacks the specific arrangement of elements including partitioning

the application specific integrated circuit into blocks (partitions), wherein each partition (block) of the application specific integrated circuit is programmed (prototyped) by programmable logic device, including connecting each partition (block) to it's own COM wrapper for converting plurality of parallel output signals to a serial data stream and back from serial data stream to the plurality of parallel output signals for communication between partitions (blocks) of the application specific integrated circuit; wherein each COM wrapper contains serializer or deserializer.

17. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

VUTHE SIEK
PRIMARY EXAMINER